(Development of) ITK DAQ & Test Setup

Any incomplete or inaccurate is solely on JZ

Introduction

- Survey what being developed and regularly discussed by such as
  - ITK Pixel Electronics group
  - ITK Pixel Readout group
  - ITK Strip DAQ group
- Develop the adequate test setups for multi module testing
- Align to the final readout system as possible

Test Setup Functionality

- Readout electrical objects
  - Single chip (FE-I4, RD53, ABC130, ABCN250, etc)
  - CMOS sensor/chips
  - Module
  - Stavelet (Strip)
  - Stave
- Readout optical objects
  - Stavelet (Strip)
  - Stave
- Readout multiple objects
  - Multiple stave system

Development Variants

- High Speed I/O (HSIO) based
  - HSIO and add-ons
  - HSIO-II and add-ons
- PCIe based
  - YARR
  - FELIX
- Other commercial board based
  - USBpix
  - SEABAS
  - Atlys
- Something I must forgot
  - GLIB
  - … …

US Institutes

WBS	Description	Institutes
6.1.7	Off-detector electronics	
6.1.7.1	TDAQ	ANL, BNL, SLAC
6.1.9	Test Setups	ANL, Oklahoma, Oklahoma St, SLAC, Stony Brook, Washington

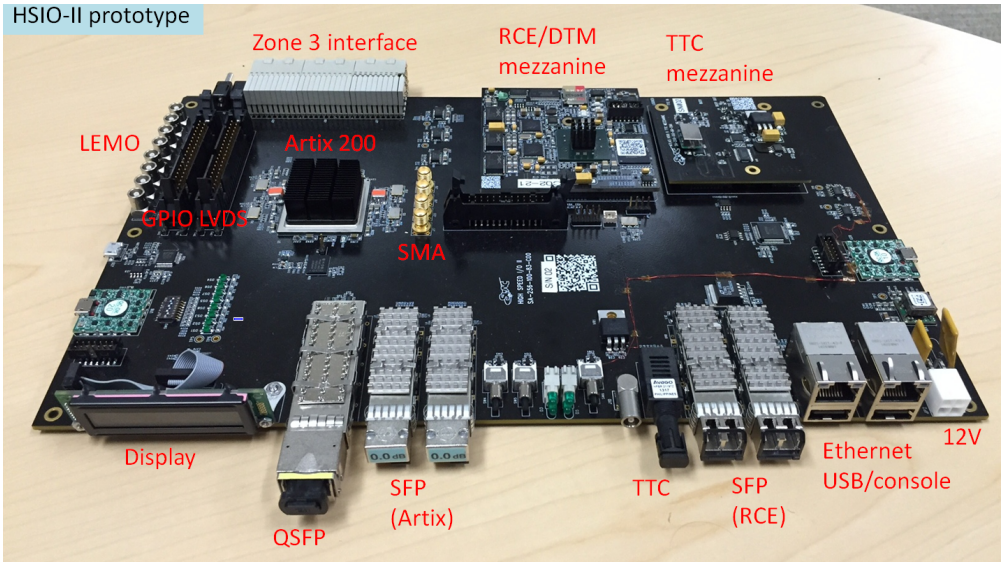
- 6.1.7 possibly to TDAQ WBS (being discussed)
- Current in PIX WBS, mainly working on development for HSIO(II) based system
  - Oklahoma State (power supply for HSIO connection), SLAC (HSIO(II)), Stony Brook (software), Washington (firmware)
- ITSDAQ development
  - Duke/ANL, started in Strip readout
- FELIX development
  - BNL/ANL, in TDAQ project

Pixel DAQ Activities (SLAC): HSIO-II / RCE

Predecessor HSIO + Gen-1 RCE served

- IBL stave loading + Q/A
- IBL connection/system tests
- Many pixel test beam setup
- Many test stands

Also ~30 HSIO serving strip upgrade test stands worldwide



⇒ *A proven concept actually does the job*

- More performant Gen-III RCE with ZYNQ is serving muon CSC readout for Run-2 operating stably since ~April.
- *Combined versatile I/O on HSIO with enhanced software programmability with RCE on DTM mezzanine in a single compact setup => HSIO-II*

Pixel DAQ Activities (SLAC): RCE/HSIO Distribution

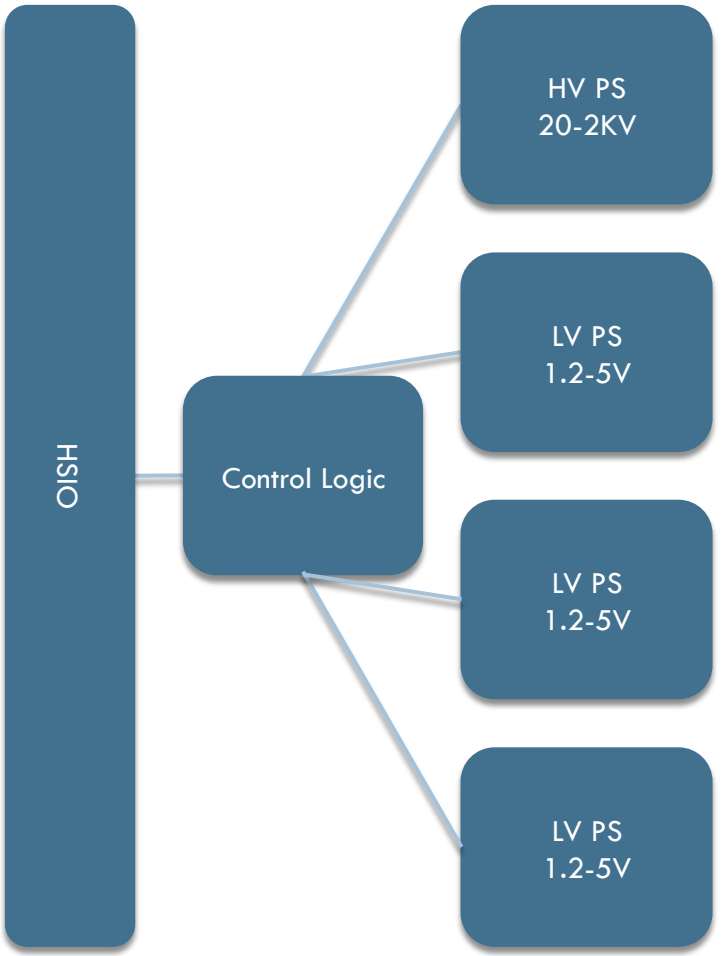
- HSIO-II prototype test verified all functionalities.
- Issues identified incorporated in new revision.
- Pre-prod two board manual loading had bizarrely many faults. Traced to misuse of a new 'superheat gun'…
- Restart at loading company (AMTECH) Jul/6 after their site move.

Institution	COB	DPM	DTM	RTM	HSIO-II	strip-interface	Pixel-interface	IBL stave interface
KEK	0	0	2	0	2	0	2	
MPI Munich	0	0	1	0	1	0	1	
Freiburg	0	0	2	0	2	2	0	
Adelaide	1	2	1	1	2	2	0	
Geneva + Bern	0	0	2	0	2	0	2	
Ljubljana + DBM	0	0	3	0	3	1	0	2
UCL (for UK 2014)	5	10	6	5	2	0	2	
UCL (for UK 2015)	1	4	4	1	2	0	2	
Gottingen	0	1	1	0	1	0	0	
Oxford (2014)	1	2	2	1	1	0	1	
Oxford (2015)	1	4	1	1	0	0	0	
IFAE Barcelona	0	0	1	0	1	0	1	
INFN Genova	0	0	2	0	2	0	2	
CERN PH-ADE-ID	0	0	2	0	2	0	1	1
BNL	0	0	1	0	1	0	1	
LBNL	0	0	1	0	1	0	1	
NYU	0	0	1	0	1	1	0	
U Illinois Urbana	0	0	1	0	1	1	1	
U Washington	0	0	1	0	1	0	1	
	9	**23**	**36**	**9**	**29**	**7**	**19**	**3**

Other components already in various stage of production.
Hoping to conclude production by early August.

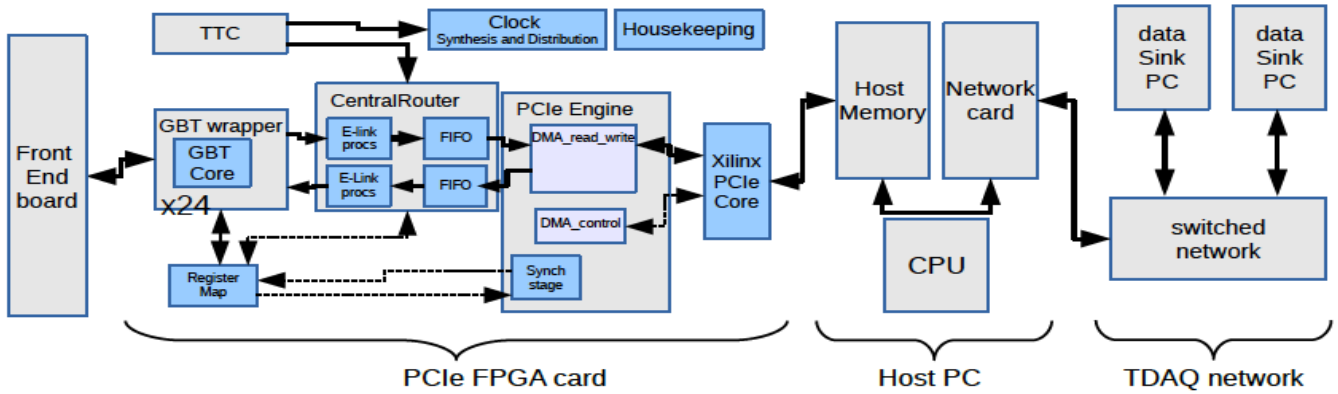
HSIO

- Oklahoma State U. group is committed to producing a power supply for Sensor Modules used with HSIO
- Steven Welch has designed a power supply capable of supplying multiple modules with HV and LV power
- Graduate student Thilak Madhuranga is developing the software interface for the power supply
- Plan to complete HSOI power supply design by the end of 2015



© Steven Welch

FELIX Firmware Development



- Developing kits and testing setup at BNL/ANL
- Initial version of firmware and software developed
- Full chain functionality demonstrated
  - **GBT transmission, TTC handling,** central router, PCIe engine, packet processing, network throughput

Proposal: ITk Pixel DAQ Prototyping

Request support from US ATLAS to support UW EE graduates

- **Common Firmware/Software development**
  - Based on pyBAR/BASIL + pit-code experience
  - Benchmark calibration performance of each HW
  - Test conceptual design of FELIX-ITk
- **Scalability Requirement**
  - Module/sensor lab test O(4)
  - Testbeam system/stave QA O(10)
  - Production system O(1000)
- **Hardware support**
  - RCE GenIII/HSIO II
  - USBPIX3
  - SEABAS2
  - YARR
  - FELIX PC/PCI E
    e.g. NETFPGA-SUME

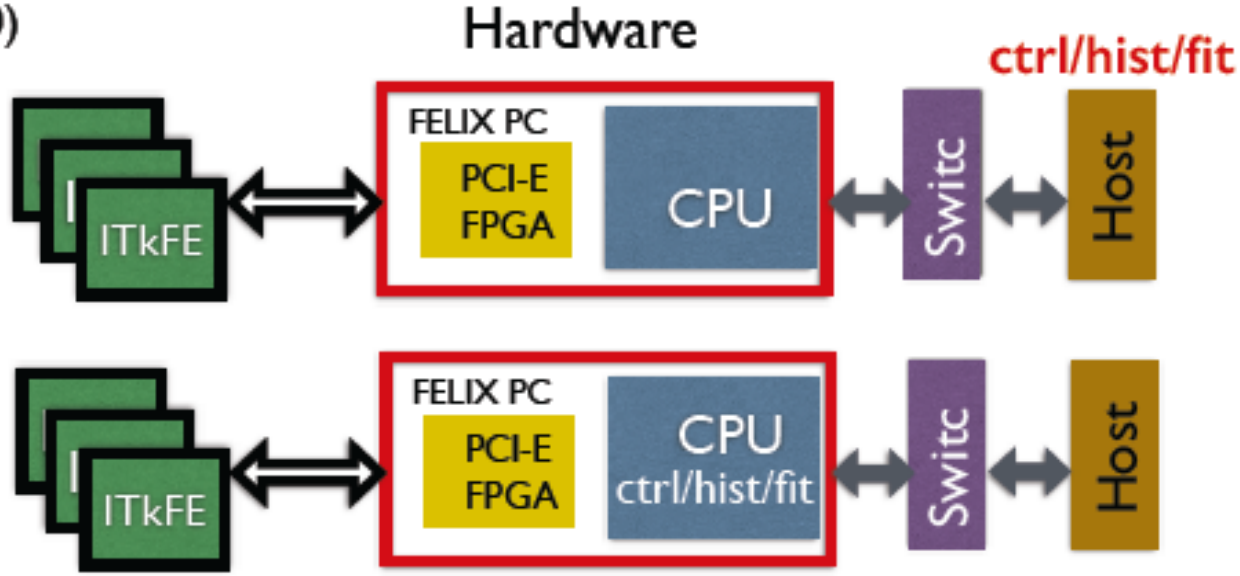
Calibration Path

FELIX-ITK I

original design: calibration control, trigger and analysis are behind the switch

FELIX-ITK II

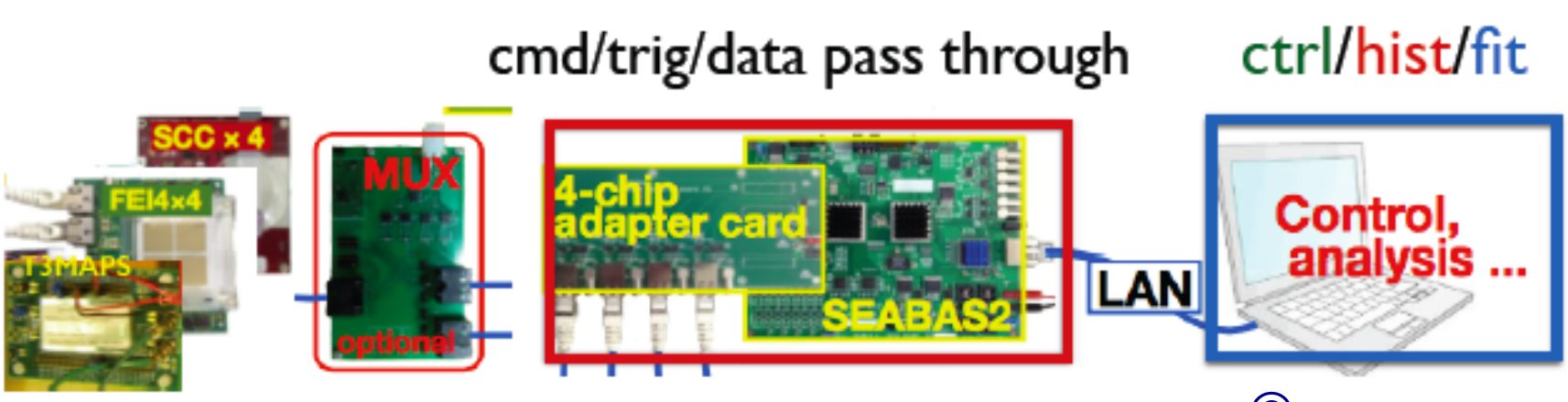
move all calibration loop to FELIX PC (maybe more realistic)



WSEABAS2, pyBAR/BASIL

- SEABAS2 : General purpose readout board with SiTCP (KEK)
- pyBAR/BASIL: Bonn ATLAS Readout system based on modular rapid DAQ development design (Bonn, UW. Hawaii, …)
- Highlight: Adopted by D3 experiment; sw support EUTelescope,
- Data taking: 4 FEI4 chip, MUX adapter, T3MAPS
- Calibration path: raw hits are all transmitted to the host PC for analysis. Permits easy access of low level information for pixel R&D.
- UW contribution (collaboration with Japan ATLAS, LBNL and Bonn)
  - Migration of Basil/pyBAR to SEABAS
  - T3MAPS readout and MUX/4-chip readout

Calibration Path



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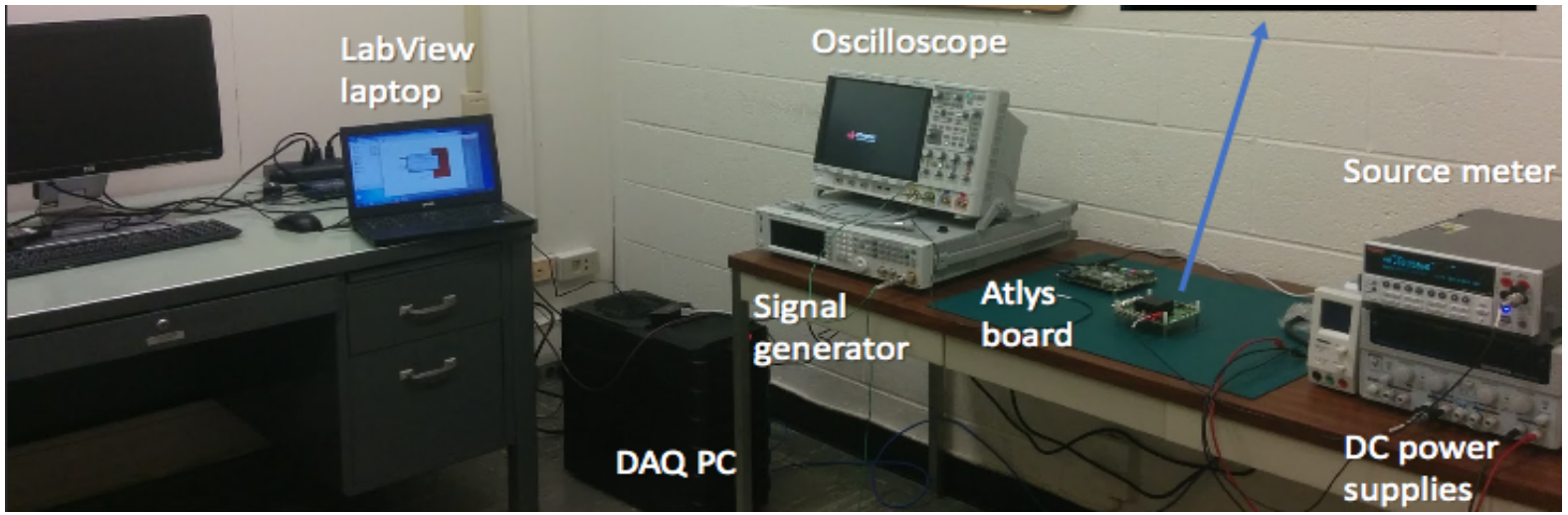
ITSDAQ Development



- Duke/ANL working on firmware for ABC and CMOS testing
- A testbed with Atlys and HVStripV1

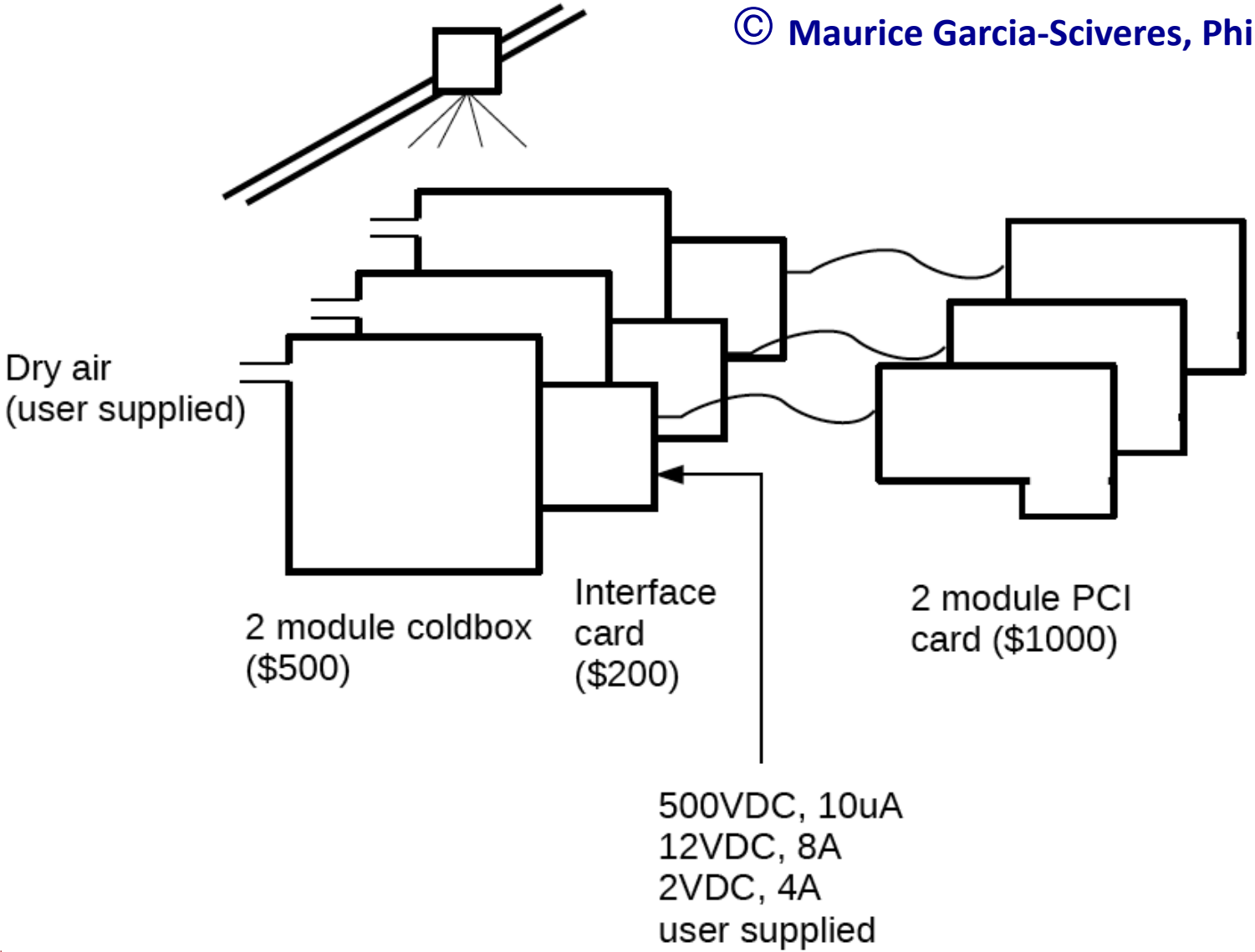
Module Production Test

© Maurice Garcia-Sciveres, Philippe Grenier

- Making a common, cheap and automated test system?
- Build test system and distribute to all testing sites.
- Parts of the test system might be provided by several groups.

Module Production Test

Source travels on rail system above test boxes (serves any number of test boxes)

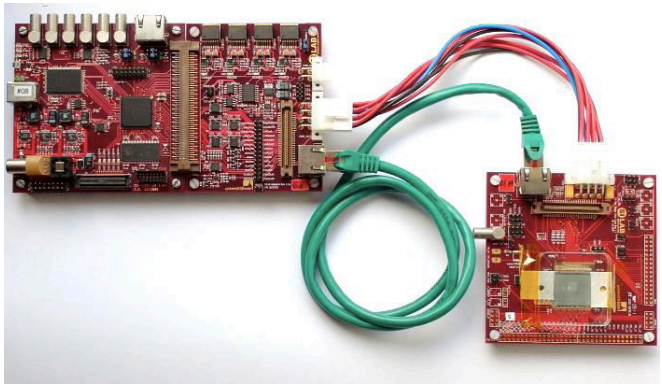


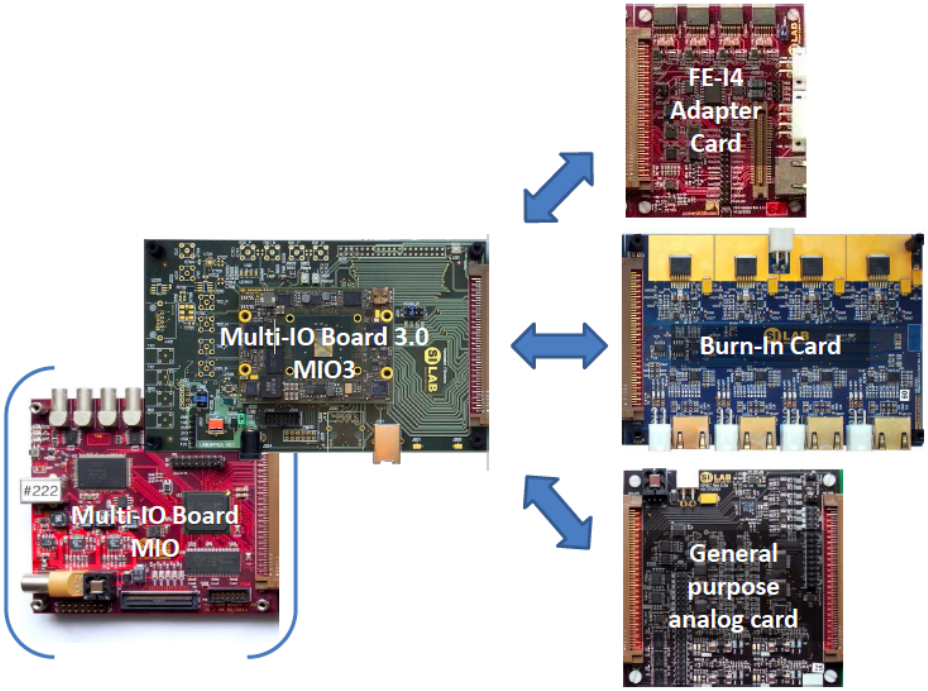
Points

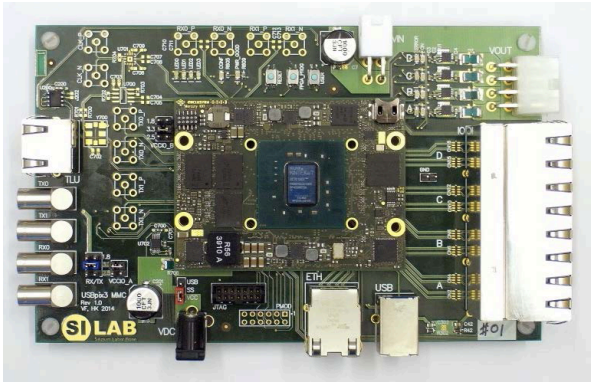
- Various test stand configurations vs same one everywhere (if ever possible, when possible)
- (common/standard) firmware and software
  - Core firmware
  - General control firmware
  - Network interface firmware
  - Readout firmware
  - TTC related firmware
  - GBT firmware
  - … …
- Testing procedures and validation
  - Across different test stands
- Full chain test setup with both electrical and optical

Stop

USBpix

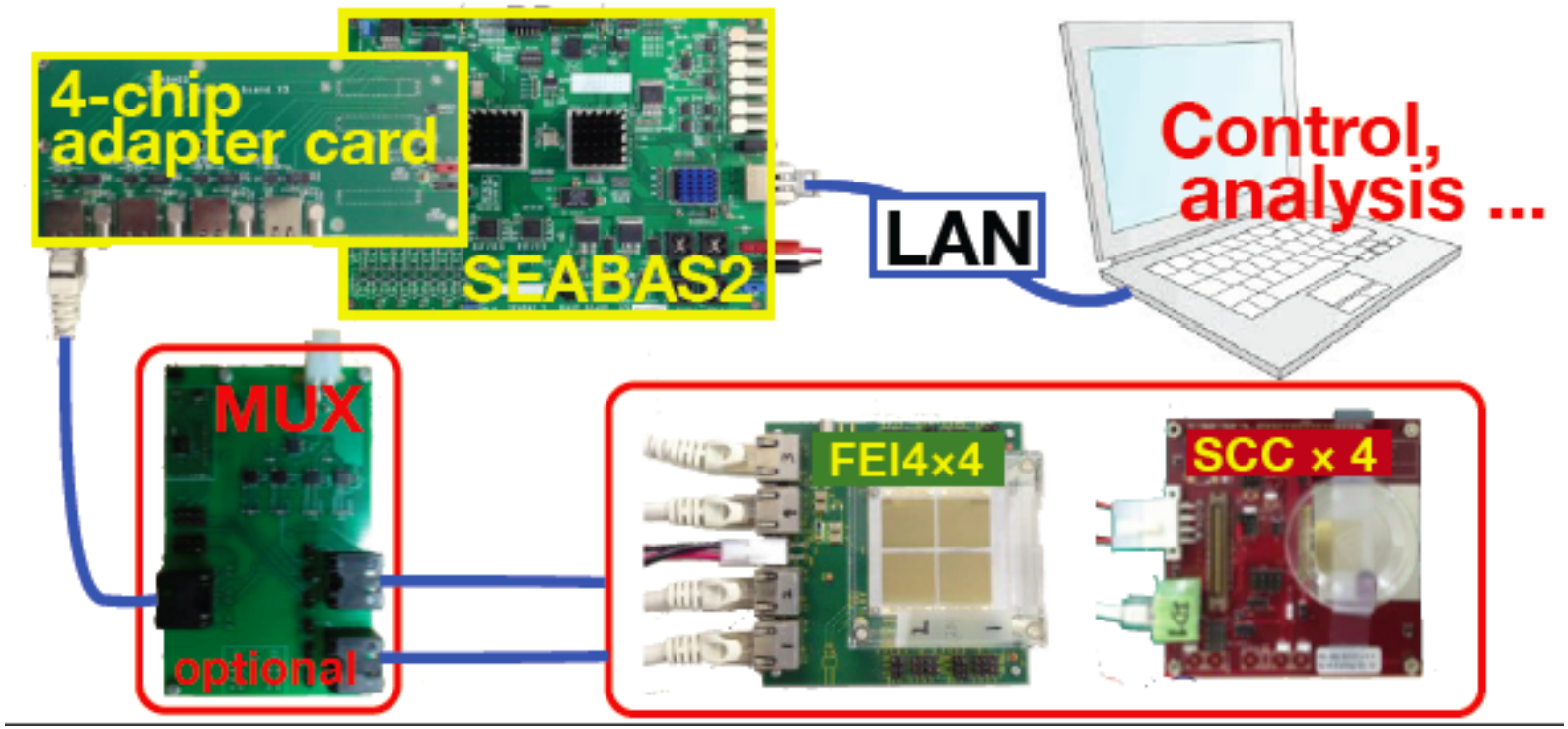






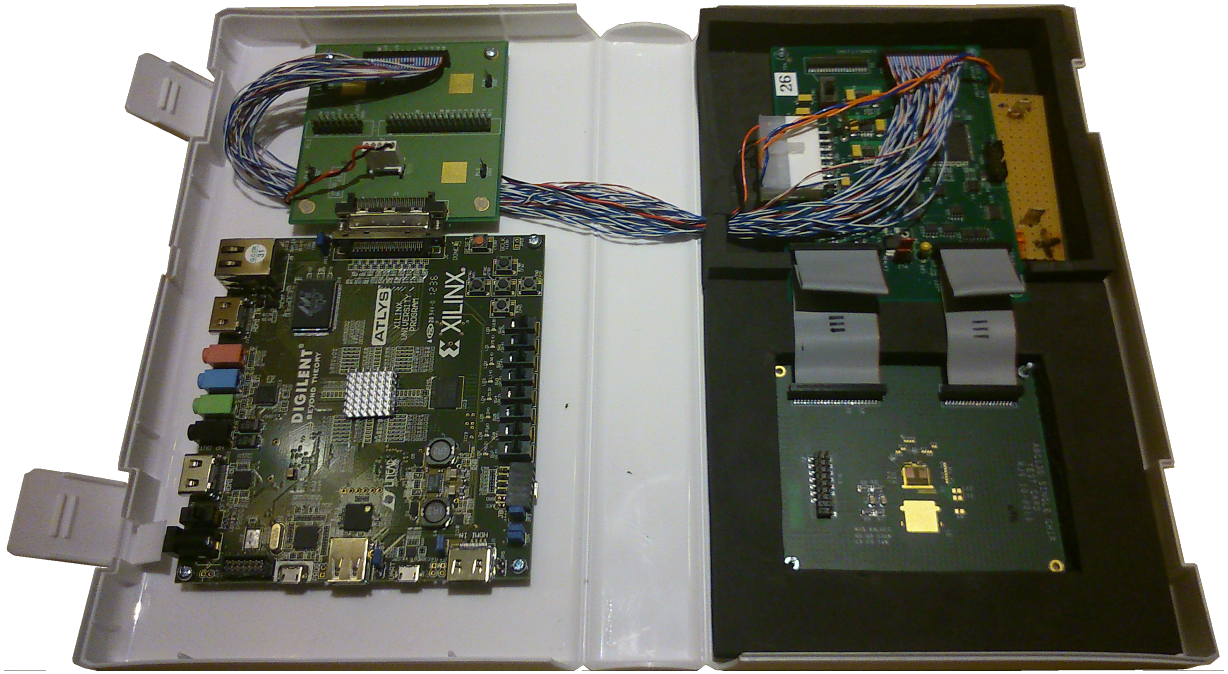
- Commercial FPGA module
- Upgrade to be compatible with existing interfaces
- Interface for CMOS testing
- Support for future PIX chips (RD53)
- Connectivity for multi-chip module/stave testing

SEABAS



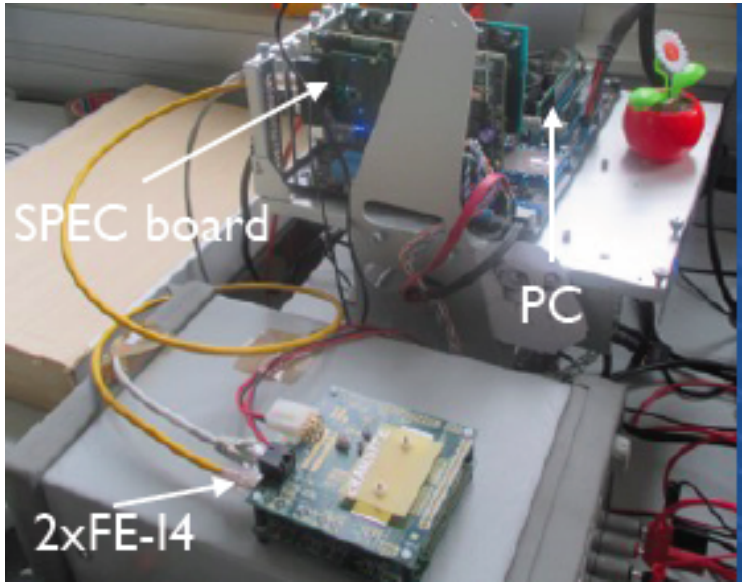
- General purpose readout board with SiTCP
- Readout up to four FE-I4s
- Used also for beam tests for ABC-130 single chip and ABCN250 super module

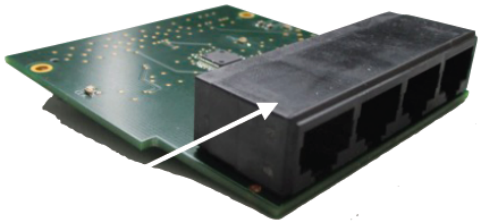
Atlys



- Digilent Atlys board with ITSDAQ
- VMOD-IB
- Driver board
- Being used also for CMOS testing
- Sufficient resources to support single-chip, hybrid and module

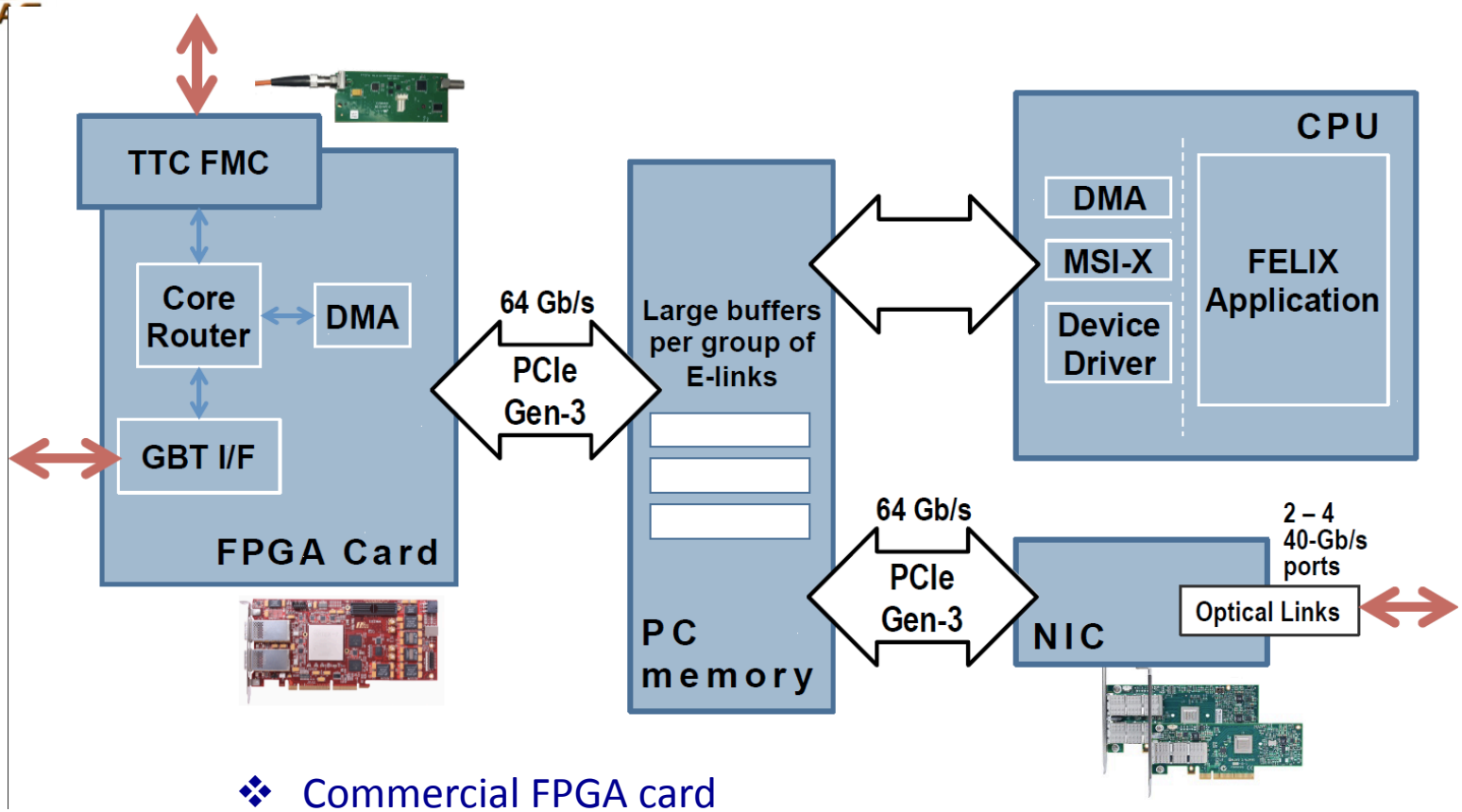
YARR





- Simple PCI Express Carrier (SPEC) Board
- Adapter board developed specifically for FE-I4

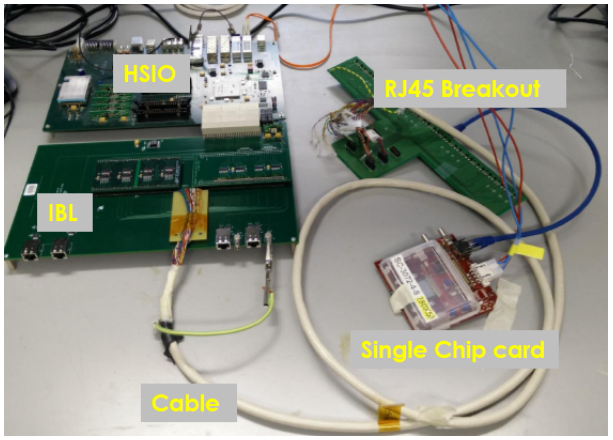
FELIX

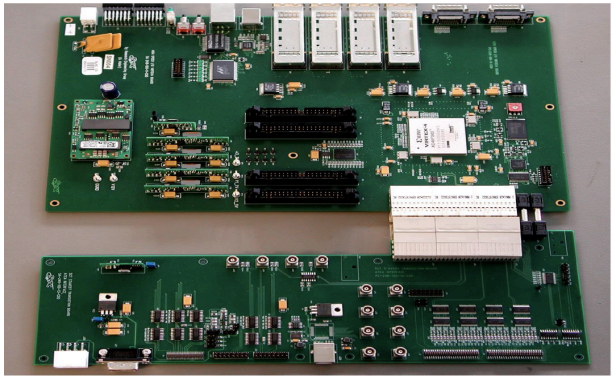


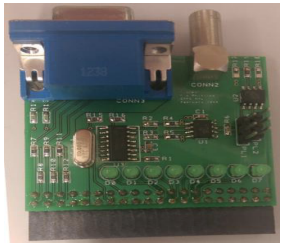
- Commercial FPGA card
- 40 Gbps Ethernet card (or 56 Gbps infiniband)
- Demonstrator with 24 bidirectional 10Gpbs links
- GBT protocol in different configurations
- TTC/BUSY handling

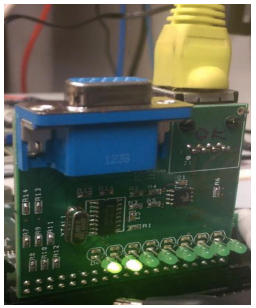
HSIO

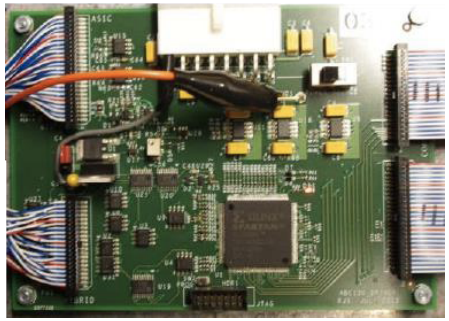
- Capacity for up to 16 FE chips
- Interface Board
  - IBL interface board
  - Si-strip interface board
  - Pixel interface board
- Add-ons
  - Clocky for programmable freq clock
  - Clucky for Interface to EUDAQ TLU
  - Driver (with interface board) – talks to ABC130 Single Chip Board



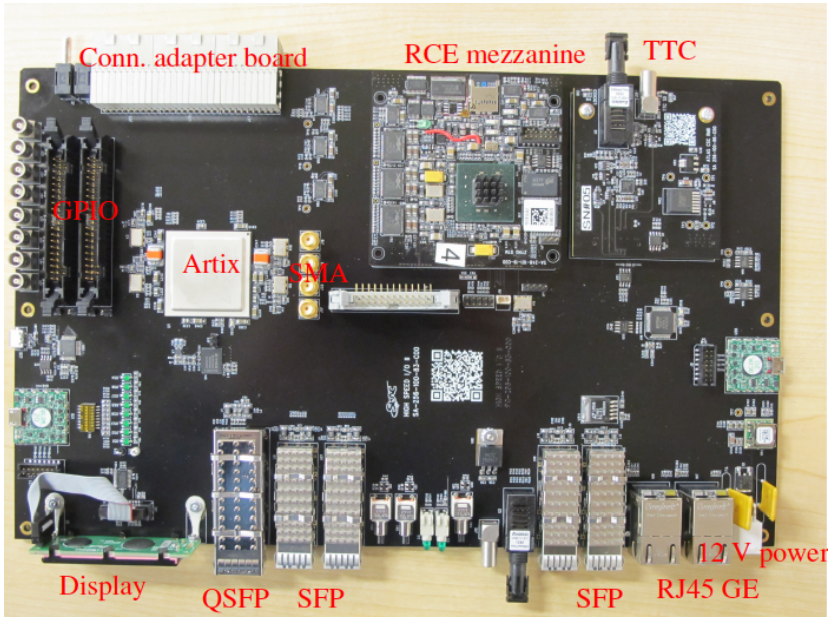


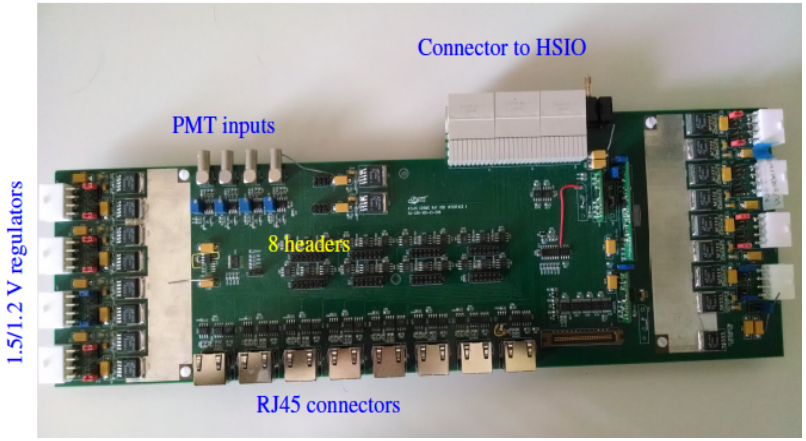






HSIO-II





- Gen-3 RCE mezzanine
- TTC mezzanine
- Adapter board with 18 (8) RJ45
- Capacity for testing of 16 FE-I4 chips